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FPGA based PWM Control for Three Phase Induction Motor

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Abstract--*The primary function of any adjustable speed motor drive is to control the speed, torque, acceleration, deceleration and direction of rotation of machine. Unlike constant speed systems, the adjustable drive permits the selection of infinite number of speeds within its operating range. Most multipurpose production machines benefit from adjustable speed control, since frequently their speed must change to optimize the machine process or adapt it to various tasks for improved product quality, production speed or safety. The control circuitin FPGA clearly has an advantage of reconfiguration over the other methods.*

Key Words- *Induction motor, VVVF, PWM, FPGA, VHDL.*

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I. INTRODUCTION

Majority of the population of motors in industry are induction motors. Some loads driven by motors does not need to operate at the same speed all the time. These types of loads offer big opportunities for saving on motor energy costs by moderating their speed according to their load [1].

This work[1] describes the successful VHDL design of digital control architecture for three phase electric drive systems. The three-phase Pulse Width Modulation (PWM) generation is the heart of the inverter system. Its main function is to control the switching sequence of the power devices according to pre-loaded instructions. Field Programmable Gate Arrays (FPGAs) are providing a path for rapid prototyping and implementation of digital systems. The VHDL model of the motor controller allows the control over the hardware implementation complexity and therefore it can be readily adapted to the available hardware resources.

Using Field Programmable Gate Array (FPGA) technology all the functions can be implemented in a single chip. The implementation tool fits the entered design into the target device. It compiles a design file into a configuration file that is optimized in terms of use of logic gates and interconnections for the target device. Design verification includes functional simulator, in circuit testing and timing simulation. The main function is to verify the proper operation of the designed circuit.

The complete development of the system has been achieved using VHDL and implemented into a single FPGA chip.

II. FIELD PROGRAMMABLE GATE ARRAY (FPGA)

A Field Programmable Gate Array is a reconfigurable digital integrated circuit that can be programmed to do any type of digital function. There are two main advantages of an FPGA over a microcontroller chip.

- FPGA has the ability to operate faster.
- FPGA supports hardware that is upwards of one million gates.

FPGAs are programmed using support software and a download cable connected to a host computer. Once they are programmed, they can be disconnected from the computer and will retain their functionality until the power is removed from the chip. The FPGAs can be programmed while they run, because they can be reprogrammable in the order ofmicroseconds.

The FPGA consists of three major configurable elements

- Configurable Logic Blocks (CLBs) arranged in an array that provides the functional elements and implements most of the logic in a FPGA.
- Input-output blocks (IOBs) that provide the interfacebetween the package pins and internal signal lines.
- Programmable interconnects that provide routing path to connect inputs and outputs of CLBs and IOBs to the appropriate network [2].

III. HARDWARE DESCRIPTION LANGUAGES (HDL)

The key advantage of VHDL when used for systems design is that it allows the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires). HDL describes hardware behavior. There are two main differences between traditional programming languagesand HDL.

- Traditional languages are a sequential processwhereas HDL is a parallel process.
- HDL runs forever whereas traditional programminglanguages will only run if directed.

IV. OPERATION OF THE INDUCTION MOTOR

When a balanced 3φ supply is applied to the stator, it gives rise to 3 φ currents and in turn flux which crosses the air gap and links the rotor. The air gap flux is of constant amplitude φ_{ag} and rotates at speed ω_s. The speed for a machine is given by

$\omega_s = 120 f / P$ rpm (1)

Where f = Stator supply frequency,

P = Number of poles

Hence the motor speed can be varied by varying the supply frequency. The operating modes of Induction motor are shown in Fig. 1.

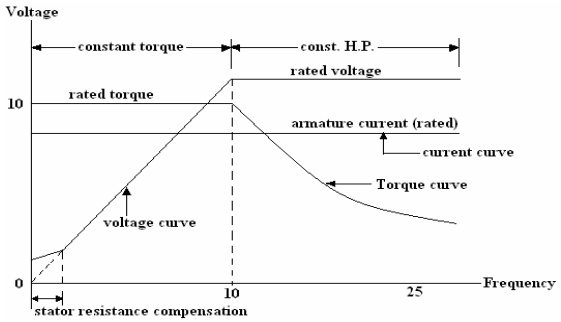

Fig. 1. Operating modes of the Induction Motor

A. Constant torque mode (below the rated speed)

Here Vs/f ratio is kept constant and frequency is varied from zero to rated frequency to vary the speed from stand stillto rated base speed.

B. Constant horsepower mode (above the rated speed)

The stator supply frequency is increased above the rated value to operate the motor at speeds greater than rated speed. Increase in the speed is accompanied by corresponding drop in motor torque.

C. Constant f_{sl} Region (higher speed operation)

The frequency is in the range of 1.2 to 2 times the rated frequency and motor approaches to its pullout torque.

V. SPEED CONTROL USING VARIABLE VOLTAGE VARIABLE FREQUENCY TECHNIQUE

The torque developed due to interaction between induced emf and the stator flux, at rated speed is given in terms of air gap flux (ϕ_{ag})and rotor current (Ir) as

$$T \alpha \phi_{ag} I_r$$

$$\text{But} \quad I_r \alpha \phi_{ag} f_{sl}$$

where f_{sl} = slip frequency

Thus $T \alpha \phi_{ag}^2 f_{sl}$ (2)

Stator voltage Vs is nearly equal to air gap emf (E_{ag}),which is proportional to ϕ_{ag}

$Vs \alpha \phi_{ag} f$

Thus $\phi_{ag} = V_s / f$ (3)

It is clear from (2) and (3) that voltage and frequency can be increased up to the rated value and variation in the speed isachieved without sacrificing the torque generated by the motor [5][6].

This technique is termed as Variable Voltage Variable Frequency control (VVVF).Torque speed characteristic with V/F control is linearized.

VI. SYSTEM BLOCKS DESCRIPTION

The entire system configuration consists of the 3□ induction motor, the inverter, and the control circuit as can beseen from block diagram (Fig.3). The system is controlled by FPGA SPARTAN 2S15 chip.

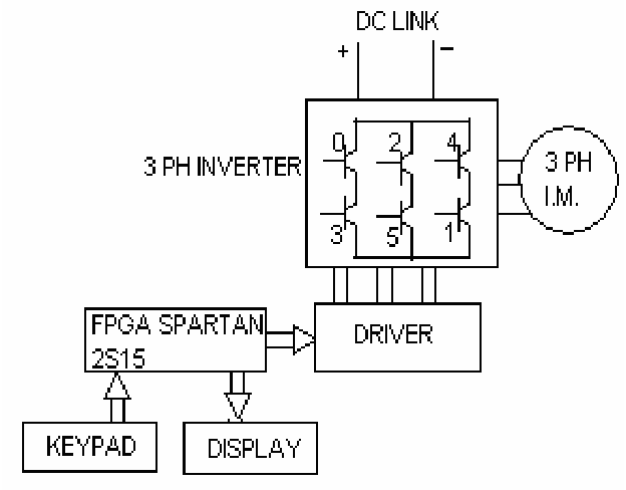

Fig. 2 System Block diagram

The mains supply is rectified using reliable bridge rectifier. The bridge rectifier provides low distortion and has an improved power factor. The rectified signal is passed on through a filter. The filter consists of both inductor and capacitor, thus giving us smooth voltage and current waveforms.

The inverter employed is a voltage source inverter. MOSFET is used as the switching device in the inverter. There are three driver cards, each card drives two MOSFET and has its own isolated power supply. This card also isolates the control and the power circuit by using opto-isolator chip. Each MOSFET is mounted on individual heat sink.

The FPGA provides the control signals to the driver card. These signals are generated according to frequency and direction defined by the user. The soft start and stop mechanism ensures proper operation of the motor. The 4x4 matrix keypad allows the user to give inputs to the system viz. frequency, direction, start, stop etc. The current frequency, speed and error messages are displayed on 7- segment LED display.

The FPGA chip provides low part count, improving reliability and almost totally eliminates the drift and electromagnetic interference (EMI) problems. It also provides flexibility of control strategy as and when needed. Any complex digital hardware can be easily implemented on the FPGA chip. It eliminates the delays generated due to programs, in case of microcontrollers /microprocessors, because of parallel operation of the digital hardware implemented on the FPGA chip [2].

The control strategy is square wave Multiple Pulse PWM to drive Inverter Bridge in 180^o mode of conduction. Devices are triggered in the sequence 0-1-2-3-4-5. The phase difference between triggering of two adjacent devices is 60^o which is incorporated by selecting 3 pulses per 60^o interval (9 pulses per half cycle). This drive results in six step waveform at the phase output. As this waveform exhibits quarter wave symmetry, all the even and the triplen (odd) harmonics are eliminated. Due to multiple switching high frequency harmonics are present but their contribution is low.

The PWM approach of control facilitates variable speed with fixed DC voltage source. PWM control suppresses harmonics and allows easy and smooth control. Thus it improves overall system efficiency [3].

VII. VHDL MODELING

A digital approach of modeling three phase pulse width modulation is presented in this paper. The three phase PWM is generated using Xilinx FPGA. Single device stay on must be avoided to prevent freewheeling current circulating, the bridge circuit that reduces the power transfer to the loadcircuit [7].

A. Synchronization and Symmetry

Three phase PWM pattern generation takes care of synchronization, three phase symmetry (TPS) and half wave symmetry (HWS)

- Synchronization: It is necessary to maintain perfect synchronization of inverter output voltage with respect to its own fundamental to avoid sub harmonics. This is possible if and only if the PWM output voltage waveform satisfies the condition given below.

$V_{RN}(\Theta \pm 2\pi) = V_{RN}(\Theta)$

$V_{YN}(\Theta \pm 2\pi) = V_{YN}(\Theta)$

$V_{BN}(\Theta \pm 2\pi) = V_{BN}(\Theta)$
where Θ is any arbitrary angle measured from the reference axis.

- Three Phase Symmetry: At low switching frequency, lower order harmonics are dominant. Three phase symmetry will ensure that all the harmonics and the fundamental of all three phases will be perfectly balanced. So triple harmonics will be cancelled from line voltage.

VBN (Θ - 2π/3) = VYN (Θ + 2π/3) = VRN (Θ)

- Half Wave Symmetry: Half wave symmetry will ensure elimination of even harmonics from output voltage. The expressions given below should satisfy to ensure HWS.

VRN (Θ ± π) = - VRN (Θ)
VYN (Θ ± π) = -VYN (Θ)
VBN (Θ ± π) = - VBN (Θ)

B. Generation of PWM Base drive

The circuit shown in Fig. 3 is used to generate the square wave having constant ON period and variable OFF period. Counter-1 produces constant ON period and counter-2 produces variable OFF period. The count for counter-1 is fixed but for counter-2 it is variable and automatically gets loaded from memory. Both the counters are 16-bit down counters. The demultiplexer selects one of the two counters depending on T-f/f output (Q). The square wave is obtainedat T-f/f output (Q-bar).

The circuit shown in Fig. 3 generates base drive pulses. The T-ff output (Q-bar) is applied as clock (clk) to this circuit This circuit produces output (OP-1) logic '1' for the 1st nine clock pulses and logic '0' for next nine clock pulses. T-f/f output (Q-bar) is ANDed with the output of this circuit (OP- 1) to produce actual Base drive signals. (Ref Fig. 5) Apositive half mains cycle is divided into sectors of 60^o, with 3pulses in each sector

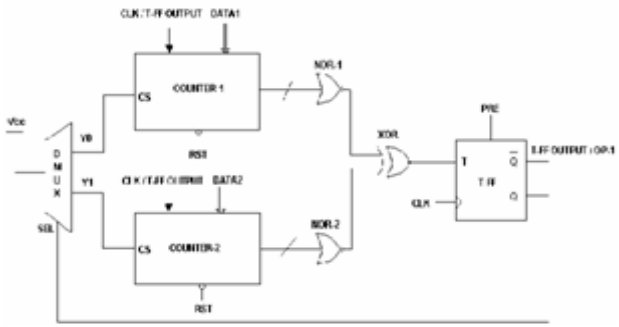

Fig 3 PWM wave generator

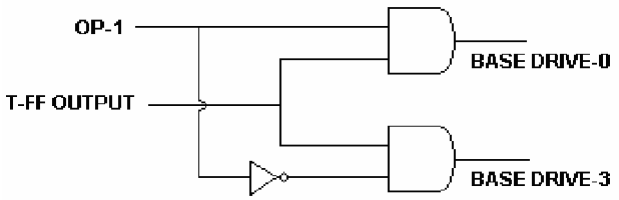

Fig. 4. Base drive generator

Three bit and six bit shift registers are used to generate base drive pulses with further phase shift of 60^o (Ref Fig. 4). Inverter logic is used to generate pulses for lower arm of the bridge.

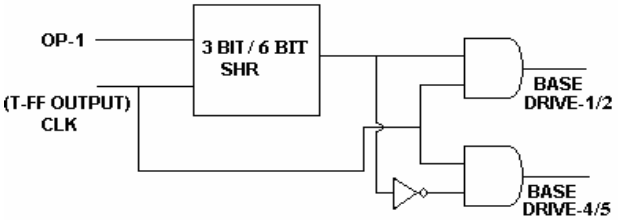

Fig. 5. Phase shifted Base drive generator

C. Base drive generation for Variable Frequency

The Fig.7 shows the interfacing of the decoder, memory and the circuit used to generate base drive pulses.

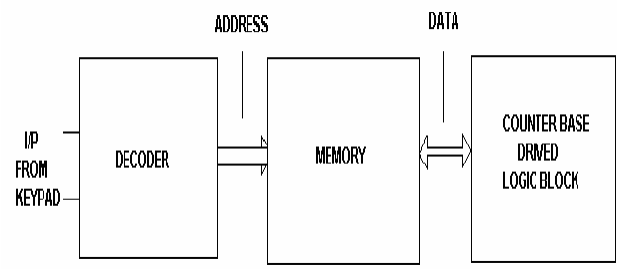

Fig. 6. Interfacing Decoder, Memory and Counter

The decoder gives address of memory location in the RAM, depending on the frequency input. The memory (RAM) size is 80 bytes. It contains the count for OFF period, which gets loaded into the counter-2 of square wave generating circuit.

The frequency reduces as the OFF time between multiple pulses is increased. Multiple values of OFF time are stored in RAM. Appropriate memory location is selected and the countis loaded in counter. (Ref Fig. 7)

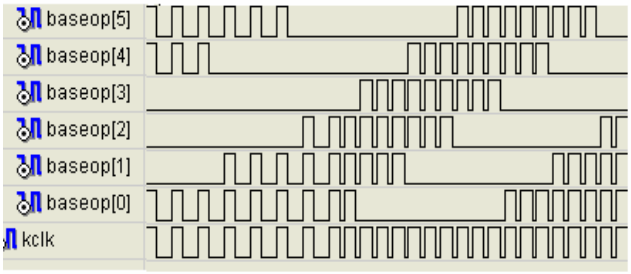

Fig. 7. Counter based drive output

D. Base drive at selected frequency, soft start and soft stop

The Block diagram shown in Fig. 9 is used to forward andreverse the motor in soft start-soft stop manner. This is achieved by comparing keyboard data and data in memory location. The frequency can be varied in the range 10Hz to 50Hz. Frequency of operation is selected using keypad. Actual frequency of rotation of motor and frequency of rotation selected by keypad are compared. OFF time between the pulses is stored in memory. This off time changes according to the difference in selected and current frequency of rotation.

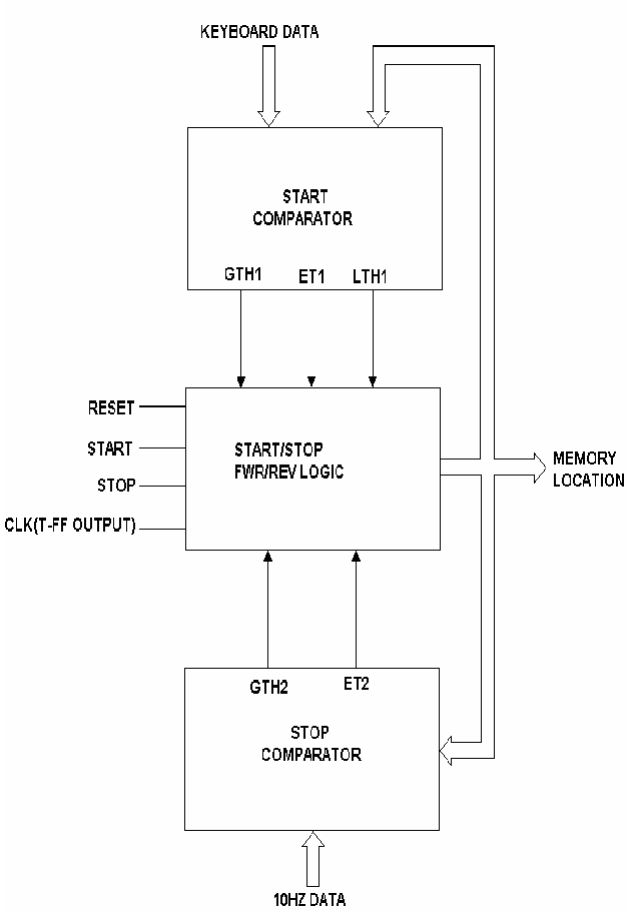

Fig. 8. Start/stop Comparator

When GTH1=1, then START COUNTER increments the current memory location. When LTH1 =1, then START COUNTER decrement the current memory location. This continues until current memory location value matches required memory location value. When ET1=1, then START COUNTER is deselected.
Soft stop and soft start action is observed when motor is rotating in forward or reverse direction and reverse or forward key is pressed respectively. Motor first stops and then start with gradual change in the pulse width.(fig 9)

	Output		
Input Condition	**GTH1**	**LTH1**	**ET1**
Keyboard data > Memory location	1	0	0
Keyboard data < Memory location	0	1	0
Keyboard data = Memory location	0	0	1

Table. 1. Logic for start stop and frequency change

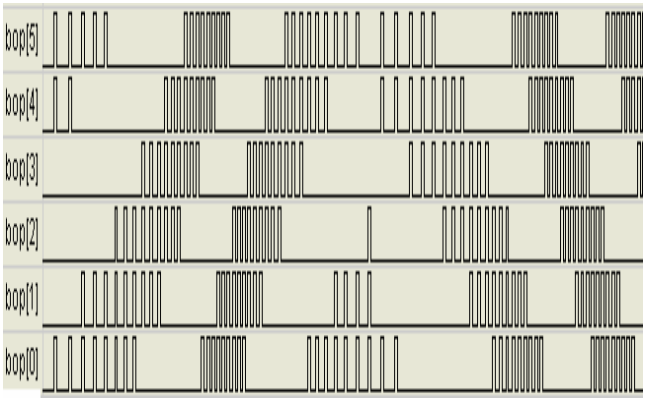

Fig. 10. Base drive waveforms during reversal of direction

VIII. CONCLUSION

Three phase ac control provide a simple and low cost option for speed control of three phase induction motor. Invention of modern fast switches as IGBT and MOSFET improves the performance of ac voltage regulators. PWM control strategy is used for speed control of three phase induction motors to improve the motor performance. FPGA is used in producing digital control for the required switching signal in efficient manner. The digital control system provides a speed control and soft starting technique for the induction motor. The digital control system provides on line controllable dead band time for the base drive pulses.

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