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Design and Development of Artix-7 FPGAbased Educational Board

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***Abstract**: This paper proposes a new approach that makes it possible for every student to perform experiments of developing and designing a board within limited time available for the course. An educational FPGA board and respective interface are also discussed. The board is a low-cost and high-performance Single Board Computer built around the Xilinx Artix-7 FPGA family XC7Z010 chip. This design provides a hardware implementation and algorithm verification platform for high-speed digital signal processing system.*
***Keywords**: Artix-7 FPGA; hardware specification; interface design; PCB.*

I. INTRODUCTION

FPGA (field programmable gate array) as a large-scale programmable logic device with lots of advantages, such as, flexible architecture and logic unit, high integration, low design cost, short design cycle, advanced development tools, high reliability, and wide scope . These advantages make it applied increasingly common in the field of digital signal processing, and widely used in product prototyping design and manufacture, thus FPGA is becoming one of the most mainstream processors [1].

This paper proposes an approach that makes it possible to perform experiments by every student within limited time for the course. The uniqueness of the proposed approach is in its strategy of guiding students toward complete understanding of designing. The approach consists of clear and completed steps, and at every step, students can verify their achievement by themselves and attain satisfaction [2].

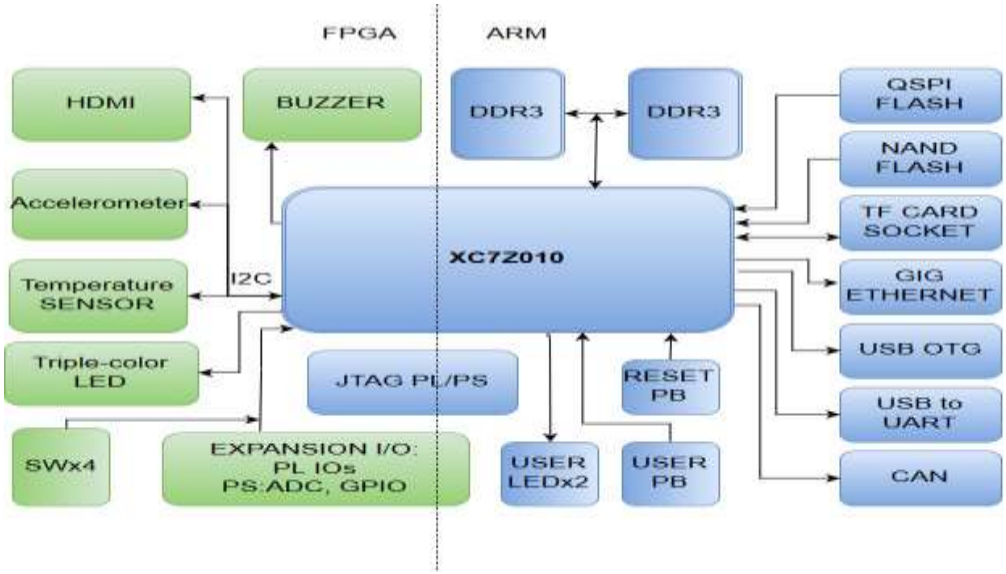

Figure.1. Block Diagram of Educational Board

To verify that the proposed approach is feasible for laboratory for students, I have designed schematic for a FPGA device using Cadence 16.6 Allegro. The design is based on Xilinx XC7Z010-1CLG400C, featuring integrated dual-core ARM Cortex-A9 processor with Xilinx 7-series Field Programmable Gate Array logic. The hardware platform has a lot of practical interfaces as shown in figure 1 block diagram of educational board, such as USB-to-UART, Mini USB OTG, 10/100/1000Mbps Ethernet, CAN, HDMI, TF, JTAG, Buzzer, G-sensor and Temperature sensor. On the rear of the board, there are two 1.27mm pitch 80-pin SMT female connectors to allow the availability of 96 for 7010 user I/O and configurable as up to 39 LVDS pairs I/O. The hardware platform is suitable for for a wide range of exercises in courses on digital logic and computer organization, from simple tasks that illustrate fundamental concepts to advanced designs and can be further developed into related products.

II. HARDWARE SPECIFICATION

1. FPGA

Artix-7 FPGA family is Xilinx's latest high performance programmable devices, using a common 28nm architecture designed for maximum power efficiency; Artix-7 FPGA density reached 28,000 logic cells [3].In this paper, taking the compatibility, scalability and cost into account, using the same FPGA in the Artix-7 series FPGA, namely XC7Z010 chip, packaged is CLG400, speed class is - 1, can support up to 12.5Gb / s of GTX. There is a FLASH memory capacity of 1G Peripheral for storing configuration and programs [4].

2. Power supply

An external USB power supply or DC 5V/2A can be used by plugging into to the power jack. The supply must use a coax, center-positive 2.1mm internal-diameter plug, and deliver 4.5VDC to 5.5VDC and at least 2.5A of current (i.e., at least 12.5W of power). Above 6VDC of power supply voltages might cause permanent damage. Information of specific currents depends on FPGA configuration and the values provided in table I are typical of medium size or speed designs.

Table I: Power Distribution

Supply	Circuits	Current (max/typical)
3.3V	FPGA I/O, USB ports, Clocks, Ethernet, SD slot, Flash, HDMI	2.5A/0.1A to 1.5A
1.0V	FPGA, Ethernet Core	2.5A/0.2A to 2.1A
1.5V	DDR3	1.2A/0.1A to 1.2A
1.8V	FPGA Auxiliary, Ethernet I/O, USB OTG	1.2A/0.1A to 0.6A
1.8V	XADC Analog	200mA/20mA
3.3V	Audio Analog	150mA/50mA

3. Memory

The board includes two Micron MT41K256M16HA-125:E DDR3 memory components creating a single rank, 32-bit wide interface and a total of 512MiB of capacity. The DDR3 is connected to the hard memory controller in the Processor Subsystem. Both the memory chips and the PS DDR bank are powered from the 1.5V supply. A simple resistor divider creates mid-point reference of 0.75V and as external reference is available to the Zynq [5].

4. Storage

The board features a 128M-bit Serial Flash. The winbond W25Q128BV is used on this board. The Multi- I/O SPI Flash memory is used to provide non-volatile code and data storage. It can be used to configure the PL subsystem (bitstream) as well as initialize the PS subsystem [6].The board provides a microSD slot for non-volatile external memory storage as well as booting the Zynq. The SD slot is a powered from 3.3V but is connected through MIO Bank 1/501 (1.8V). Therefore, a TI TXS02612 level shifter performs this translation. The TXS02612 is actually 2-port SDIO port expander, but only its level shifter function is used. The slot is wired to Bank 1/501, including Card Detect. On the PS side peripheral SDIO 0 is mapped out to these pins and controls communication with the SD card. The peripheral controller supports SD transfer modes 1-bit and 4-bit, but does not support SPI mode. Based on the Zynq TRM, SDIO host mode is the only mode supported [7].

5. Communications

The board uses an Atheros AR8035 PHY to implement a 10/100/1000 Ethernet port for network connection. The PHY connects to MIO Bank 501 (1.8V) and interfaces to the Zynq-7000 AP SoC via MDIO for management and RGMII for data. The auxiliary interrupt (INTB) and reset (PHYRSTB) signals connect to PL pins to be accessed via EMIO [8].A Microchip USB3320 USB 2.0 Transceiver Chip with an 8-bit ULPI interface is used as the physical layer (PHY). The physical layer (PHY) features a complete HS-USB Physical Front-End supporting speeds of up to 480Mbs. The USB OTG interface can act as an embedded host or a peripheral device [9].The board includes a CP2103 USB-UART bridge for using PC applications to communicate with the board using standard Windows COM port commands. Serial port data is exchanged with the Zynq using a two-wire serial port (TXD/RXD). I/O commands can be used from the PC directed to the COM port to produce serial data traffic on the pins of Zynq. The port is tied to pins of PS (MIO) and can be used in combination with the UART controller. A 3.3V->1.8V voltage level translation interfaces the CP2103 with MIO Bank 501, a process transparent to the user [10].

6. Display

An input and output-capable of HDMI Port connects to the programmable logic pins. Over this connector an HDMI or DVI-compatible video stream can be driven in or out of the board. Encoding or decoding the HDMI video stream needs to be implemented in logic, as well as auxiliary functions, like DDC or CEC.

Depending on the actual design, it can take the Source role driving a monitor/TV display, or behave as a Sink accepting a video stream from any HDMI Source, like a laptop or smartphone. It supports resolution up to 1080p.

7. User I/O

There are two 1.27mm pitch 80-pin SMT female connectors on the rear of the board to allow the availability of 96 for user I/O and configurable as up to 39 LVDS pairs I/O.

8. GPIO

The board includes a four channel toggle switch, two push buttons for a Reset and Userand five individual LEDs connected to the Zynq PL, three are User LEDs, one is power indicator and one RGB LED. The pushbuttons and slide switches are connected to the Zynq via series resistors to prevent damage from inadvertent short circuits. The pushbuttons are "momentary" switches that normally generate a high output only when they are pressed and a low output when they are at rest. Slide switches generate constant high or low inputs depending on their position. The board consist a three-axis acceleration sensor and temperature sensor The board is configured to boot in Cascaded JTAG mode, which allows the PS to be accessed via the same JTAG port as the PL. It is also possible to boot the board in Independent JTAG mode by loading a jumper and shorting it. This will causeonly the PL will be visible in the scan chain and the PS to not be accessible from the onboard JTAG circuitry. To access the PS over JTAG while in independent JTAG mode, users will have to route the signals for the PJTAG peripheral over EMIO, and use an external device to communicate with it.

9. PCB design

Since this design is high-speed signal processing board, so signal integrity problems are considered. Using Cadence Allegro PCB Editor software to do the before and after wiring simulation on key high-speed lines, can be predicted signal transmission conditions and overall system performance, thereby enhancing the reliability of the system. The stackup in the design of the board PCB are a total of 8 layers, there are 4 signal layers, 2 GND layers and 2 power planes, respectively. It is not recommended to have more than two adjacent signal layers between the planes as this creates impedance discontinuities and increases crosstalk between these signal layers.Two plane layers are added to the centre of the substrate that result into tight coupling between the centre planes and isolates each signal plane reducing coupling and crosstalk dramatically. This configuration is commonly used for high speed signals of DDR2 and DDR3 designs where an issue of crosstalk due to tight routing.

III. CONCLUSION

Using FPGA as prototyping platforms, this board will take students through a typical SoC design process from creating high-level functional specifications to design, implementation and testing on real FPGA hardware using standard hardware description and software programming languages.

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