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Implementation of Double Integrated Buck Converter.

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Abstract :*In buck converter the narrow duty cycle limits the step down dc-dc conversion. This limitation can be overcome by using double integrated buck converter providing high power factor and output current regulation. The high step down capability and output current regulation is provided on the integration of tapped buck dc/dc converter. This suits for medium power solid-state light applications. The hardware representation and simulation of a circuit with 230 V input and 60 V/500 mA output has been done and verified by MATLAB. The proto type model of double integrated buck converter was developed and tested and the result are Satisfactory.*
Keywords - *Controller, DC-DC Converter, DIBC, High Step Down, Rectifier.*

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I. INTRODUCTION

A buck converter steps down voltage from its input to output. It is a dc- dc power converter which comes under switched mode power supply. The switched mode power supply consists of atleast two semiconductors (diode and transistor or two transistors) and a storage element.

LED lamps which require lower energy and maintenance cost with a longer life uses the double integrated buck converter to provide the required input voltage[1]-[4]. This scheme also eliminates the use of electrolytic capacitors. LED's are used in consumer electronic products in a wide range. The double integrated buck converter doesn't require any output inductive filter because of the presence of capacitor filter which helps in clamping the rectifies diode voltage[5]-[8].

The double integrated buck converter also provides high power factor correction and output current regulation improving safety and make use of film capacitors rather than electrolytic capacitors. This enhances the overall ballast robustness[9]-[10]. The converter duty cycle is decreased by the feedback control loop to regulate the output and keeps the LED current constant. So that the input power also decreases. [11]-[12].

II. DIBC

The double integrated buck converter consists of an ac supply, filter, rectifier, DIBC, load and controller. Initially an input ac voltage of 230V is fed into the system .This input voltage is sent to the rectifier after filtering unwanted distortions by using a filter. From the filter the ac supply reaches the rectifier where it gets converted into dc.

The conversion of alternative current to direct current is known as rectification since it straighten the direction of current. For example vacuum tube diodes, mercury arc valves, semiconductor diodes, silicon controlled rectifiers and other silicon based switches. The double integrated buck converter overcomes the limitation of a buck converter.This provides high power factor and output current regulation. A DIBC uses offline power supply for LED lighting based on the integration of a buck power factor corrector and the tapped buck DC-DC converter having high step down capability and output current regulation.

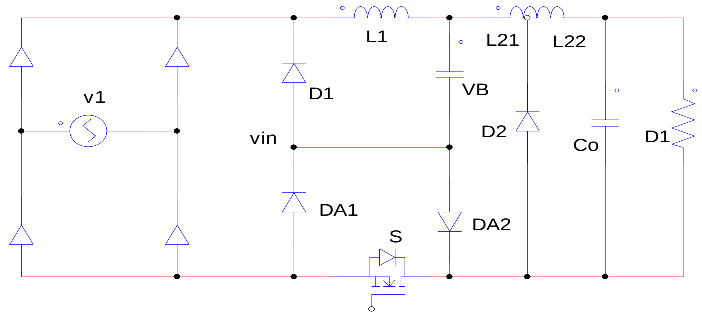

Fig 1

III. OPERATION

The DIB converter behavior, it is worth analyzing its operation at a given instant within the line conduction angle $[\theta_1 < \theta < \pi - \theta_1]$. The output semi-stage tapped inductor is modeled through a mutual inductor with series-connected windings where the magnetizing inductance L_2 has been reported at the secondary side.

To simplify the analysis, some preliminary assumptions can be done. In particular, the DIB converter is supposed to operate at steady state, all component non idealities are neglected and finally, the voltage levels across the input, bus, and output filter capacitors are considered to be constant within the whole switching period. Assuming four different intervals can be identified within the converter switching period, involving four of the five topological phases that can possibly occur.

Interval I

Phase 1$[t_0 = 0, t_1 = D/f_{sw}]$

The first topological phase corresponds to the interval during which the converter con-trolled switch S is turned on, whereas both freewheeling diodes $D_1$and $D_2$are reverse biased. During such interval, the input line energy is partly stored in converter's inductors and partly delivered to the load.

As it can be observed in the waveforms reported in Fig. 4, both inductor currents are linearly increasing according to

$i_1(t) = ((V_{in}-V_B) /L_1)t$ and $i_{L2}(t) = ((V_B-V_O) / \Lambda L_2)t$

whereas the converter output current is given by

$i_O(t) = i_2(t) = i_{L2}(t) -(N_1-N_2)\, i_2(t) = i_{L2}(t)/ \Lambda$

where Λ is a dimensionless parameter, depending on the num-ber of turns of the tapped inductor primary and secondary windings (N1 and N2), which is defined as follows: $\Lambda = (N_1+ N_2)/ N_2$ Which of the auxiliary diodes D_{A1} and D_{A2} is actually con-ducting will depend on the relationship between the currents referred to as i_1 and i_2 in Fig. 3. The two possible paths have been represented in dashed line

When $i_1 > i_2$, the bus current will flow through D_{A2}; otherwise, the recycling path is provided by D_{A1}. In the D_{A2}; otherwise, the recycling path is provided by D_{A1}. In the equal to i_1, i.e., $I_S(t) = i_1(t) = ((V_{in}-V_B) /L_1)t$ whereas it will correspond to i_2 in the latter case, i.e.,

$i_S(t) = i_2(t) =(i_{L2}(t)/ \Lambda) = (U_{22}/ \Lambda.L_2)t) = ((V_B-V_O) / \Lambda.L_1)t)$

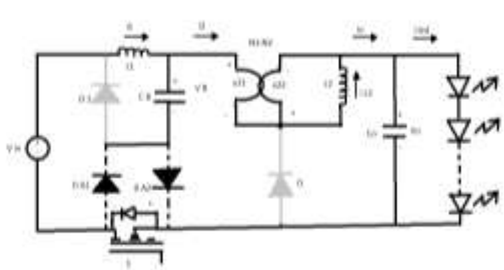

Fig 2

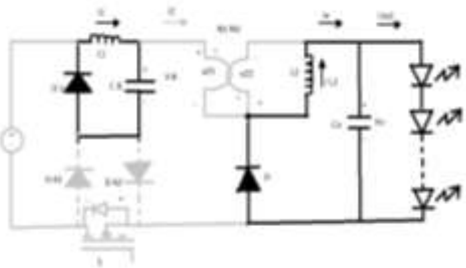

Fig 3

Interval II

Phase 2 $[t_1 = D/f_{sw}, t_2]$

During this second phase, both converter inductors are thus discharging, and their linearly decreasing currents recycle through the corresponding freewheeling diodes, i.e.,

$i_{D1}(t) = i_1(t) = (V_{in}-V_B / f_{sw}.L_1)D) = (V_B / L_1)(t-(D/f_{sw}))$

$i_{D2}(t) = i_{L2}(t) = (V_B-V_O / \Lambda.f_{sw}.L_2)D) = (V_O / L_2)(t-(D/f_{sw}))$

Both auxiliary diodes D_{A1} and D_{A2} are reverse biased, namely, $u_{DA1}= V_{in}$and $u_{DA2}=V_O(\Lambda - 1) + V_B$. The switch voltage stress is equal to $u_S= u_{DA1}+ u_{DA2}= V_{in}+ V_B+ V_O(\Lambda - 1)$

This phase ends when the current through one of the inductors reaches zero. Depending on which of the inductor currents($i_{L1} = i_1$ and i_{L2}) reaches zero first, two different topological stages can actually occur.

Interval III

Phase 3[t_2, t_{3A}]

If the current flowing through the input stage inductor reaches zero first. As it can be noticed, the converter is still disconnected from the utility grid, whereas the output stage freewheeling diode keeps delivering the tapped inductor discharging current to the output filter capacitor and to the LED load. Since the voltages on the auxiliary diodes are equal to $u_{DA1} = V_{in} - V_B$and $u_{DA2}= V_B+V_O(\Lambda - 1)$, respectively, the volt-age stress on the main switch actually results to be $u_S= u_{DA1}+ u_{DA2}= V_{in}+ V_O(\Lambda -1)$

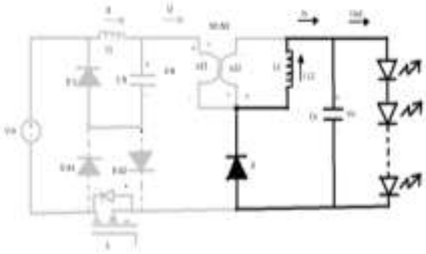

Fig 4

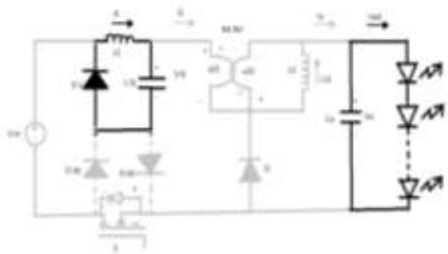

Fig 5

Phase 4[t_2, t_{3B}]

If, on the other hand, it is the tapped inductor magnetizing current to reach zero first, the corresponding topological stage. The converter is disconnected from the line, whereas the LED load is actually fed by the output filter capacitor only.The current of the input semi-stage inductor recycles through the corresponding freewheeling diode.

The voltages on the auxiliary diodes within this phase are respectively

$u_{DA1} = V_{in}$ and $u_{DA2} = V_B-V_O$,

so that the controlled switch voltage is equal to $u_S= u_{DA1}+ u_{DA2}= V_{in}+ V_B - V_O$

Interval IV

Phase 5[t_{3A} or t_{3B} ,T_{sw}]

The last phase, during which all devices are switched off, begins when both inductor currents have reached zero. As it can be noticed by inspection of Fig. 3(e), the output capacitor only actually results to be responsible of supplying the LED load within this interval until the end of the switching period.

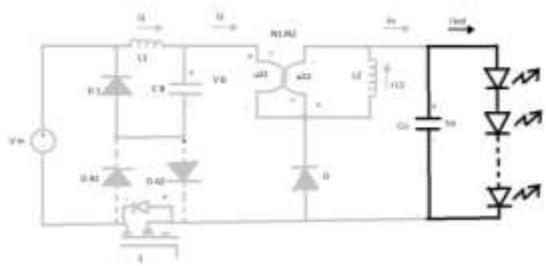

Fig 6

As concerns the stress levels, the voltages on the auxiliary diodes will be respectively equal to $u_{DA1} = V_{in}-V_B$ and $u_{DA2}= V_B - V_O$, so that the voltage stress on the main switchwill actually be

$u_S= u_{DA1}+ u_{DA2}= V_{in} - V_O$

The parameters are used to analysis the approximate values of the components and parameters. This is the operation of DIBC.

Converter Parameters	**Symbol**	**Value**
Switching frequency	FSW	100kHZ
Bus voltage	VB	160V
PFC Choke	L1	1mH
Bus Capacitance	CB	30µH
Converter duty cycle	D	0.42
Tapped inductor magnetizing inductance	L2	90mH
Tapped inductor ratio	Δ	3.85

Tapped inductor Turns ratio	N1 ⁄ N2	2.85
Ripple transformation factor	V	0.038
Output capacitance	Co	50µH

Table 2.1

IV. SIMULATION

The simulation of double integrated buck converter of high step down capabilityand output current regulation has been simulated. An input voltage of 210V and switching frequency of 100 kHz is chosen and an output of 12V/500mA is obtained.

From the input voltage and current waveforms, the resulting actual power factor is 0.92 to achieve good voltage regulation closed loop control methods used. The duty ratio linearly modulated to reduces the error in PWM control.From the output voltage and current of the new converter is 30V and 0.5A respectively. The current through the first filterinductor, tapped inductor primary winding, Freewheeling diodes, secondary winding and magnetizing inductance and also shows the active controlled switch waveform.

Current through auxiliary diodes, inductor in not similar to the tapped inductor primary side. On the other hand, to remove DA2 one inductor is lower than the other. The line regulation at Vin = 210 V.

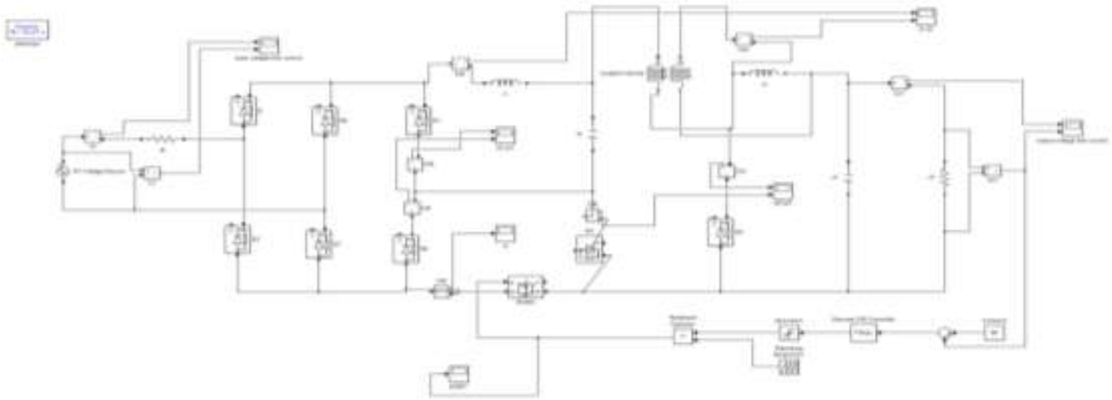

Fig 7

INPUT VOLTAGE AND CURRENT

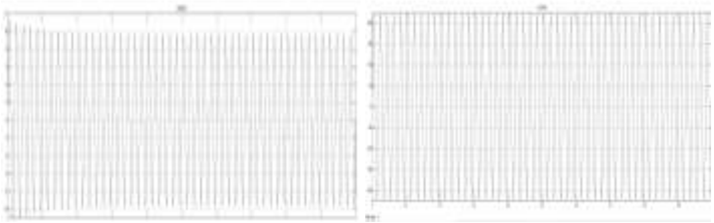

Fig 8

OUTPUT CURRENT AND VOLTAGE

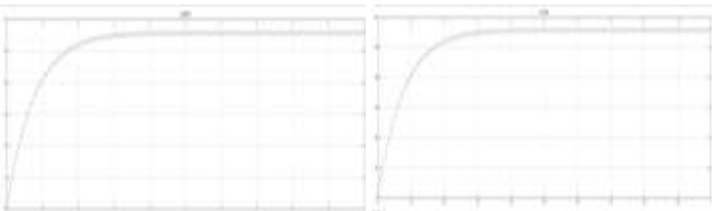

Fig 9

PULSE

Fig 10

CURRENT THROUGH D_1,DA_1

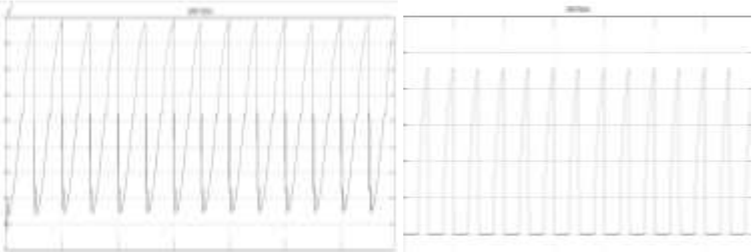

Fig 11

CURRENT THROUGH D_2,DA_2

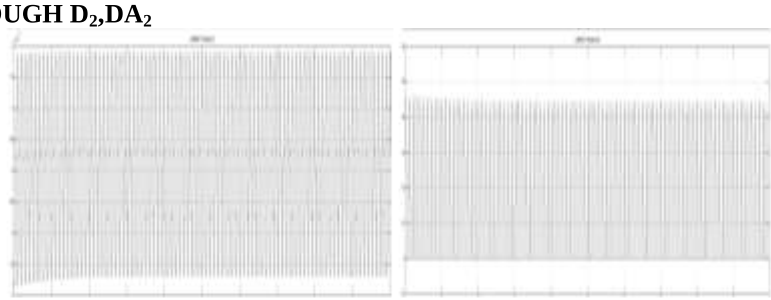

Fig 12

CURRENT THROUGH L_1,L_3

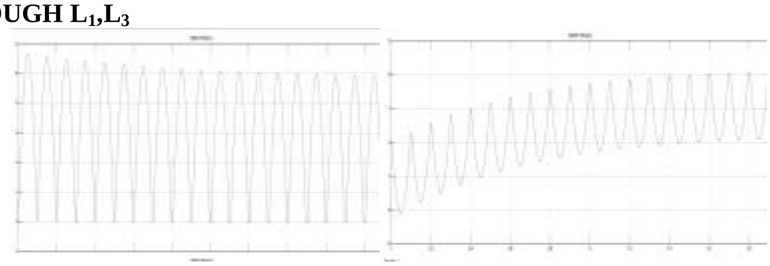

Fig 12

CURRENT THROUGH SWITCH

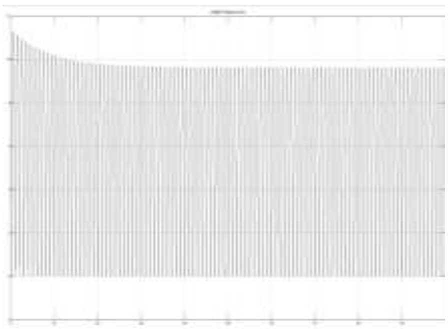

Fig 13

HARDWARE

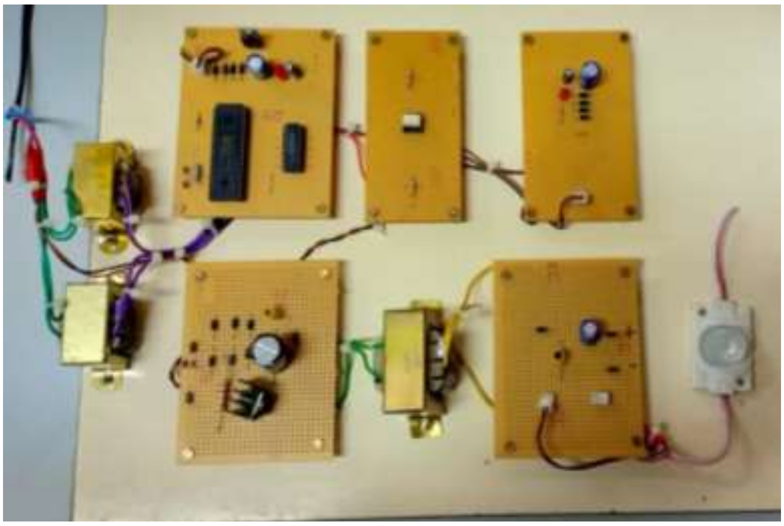

Fig 14

INPUT AND OUTPUT DISPLAY

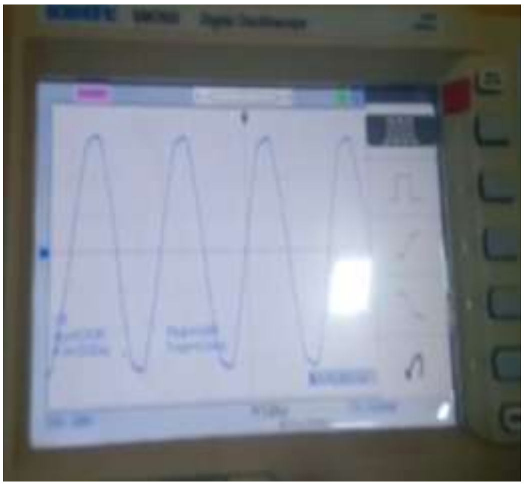

Fig 15

Fig 16

V. CONCLUSION

The closed loop control of double integrated buck converter's applications is discussed. The double integrated buck converter mainly depends on the integration of a buck power factor control with tapped buck dc-dc converter. The proposed solution provides much better control of input power factor and low frequency LED current ripple factor. When compared to other solutions. The proposed system is more simple, provides high PFC and accurate output current regulation, improving safety and robustness. This also avoid using short lifetime electrolytic capacitors. The operation principles performance of input and output semistages are analysed carefully. The simulation of DIBC with high stepdown capability, output current regulation and high power factor is done and compared with the hardware implementation. The proposed system provides an output 30 V/500mA when an input voltage of 230 Vwith a switching frequency of 100kHz is given.

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